REMARKS

Claims 1-47 are pending. Claims 13 and 16-47 are rejected. Claims 1-12, 14, and 15 are withdrawn from consideration.

Independent claims 13, 28, and 37 have each been amended to recite that caching is at chip or sub-chip resolution. The application as originally filed provides support for this feature. The paragraph beginning at page 8, line 21, states that "In digital signal processing the fundamental time unit is ordinarily the over-sampling rate of the originally transmitted signal." This same paragraph also states that "In a typical spread spectrum system, the fundamental unit of time is the chip rate." To a person of ordinary skill in the spread spectrum communication art, over-sampling of a spread spectrum signal means that the timing resolution of the resulting samples is at sub-chip level when the over-sample rate is more than 1 and at chip level when the over-sample rate is 1. Thus no new matter has been added.

Applicant has also amended some of the claims to better define the invention.

Turning to the prior art rejection, claims 13 and 16-47 remain rejected under 35 USC 103(a) as being unpatentable over Belotserkovsky et al. (U.S. Patent No. 6,621,857; hereinafter "Belotserkovsky") in view of Frank et al. (U.S. Patent No. 6,731,622; hereinafter "Frank") and Schuster et al. (U.S. Patent No. 6,591,355; hereinafter "Schuster").

Amended independent claim 13 recites "A time-sliced processor ... comprising: a data cache configured to receive input data and to cache intermediate data *at chip or sub-chip resolution* ..." Claim 13 also recites that each of a plurality of signal processing elements has "a cache configured to receive data from the data cache and to cache intermediate data *at chip or sub-chip resolution.*"

Schuster is directed generally to a method for controlling and managing Distributed Shared Memory (DSM). As stated in column 1, lines 24-27, "the DSM is typically implemented as a middleware layer, between the operating system and user applications running on host processors

that are linked by a local area network (LAN)." Further, Schuster discusses in column 1, lines 31-32, controlling access to the shared memory by different applications running on the different processors (or hosts).

Schuster does not cache at chip or sub-chip resolution, as required by the claimed invention. Data caching at chip or sub-chip resolution is essential to the claimed time-slice processing which pauses an on-going processing at a time slice boundary, switches to another processing task, and subsequently resumes the initial processing task by reloading the data in cache. Also, in contrast to Schuster's system, the claimed cache is accessed by a single computing device rather than multiple devices via a local area network (LAN). Therefore, Schuster does not teach or suggest data caching as claimed. Belotserkovsky and Frank fail to make up for Schuster's deficiencies.

Thus, independent claim 13, along with their dependent claims, is patentable over the applied references for at least these reasons.

Amended independent claim 28, similar to claim 13 discussed above, recites "A master control unit in a time-sliced processor ... wherein the master control unit is configured ... to control the data cache to cache *at chip or sub-chip resolution.*" Thus, independent claim 28, along with their dependent claims, is patentable over the applied references for at least the same reasons as discussed above with respect to claim 13.

Amended independent claim 37, also similar to claim 13 discussed above, recites "A time-sliced processor ... comprising ... a data cache for receiving input data and for caching intermediate data *at chip or sub-chip resolution.*" Claim 37 also recites that each of a plurality of signal processing means has "a cache for receiving data from the data cache and for caching intermediate data *at chip or sub-chip resolution.*" Thus, independent claim 37, along with their dependent claims, is patentable over the applied references for at least the same reasons as discussed above with respect to claim 13.

Reconsideration and withdrawal of the prior art rejection is therefore respectfully requested.

In view of the above, Applicant believes the pending application is in condition for allowance.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

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Respectfully submitted,

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